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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,925	09/01/2000	Nikhil Vishwanath Kelkar	NSC1P181/P04767	7254

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/653,925	Kelkar et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 23, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3, 5-7, 15-17, and 19-28* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3, 5-7, 15-17, and 19-28* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-7, 15-17 and 19-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US Pat. 6081026) in view of Akagawa et al (US 5834844) and the admitted prior art (APA).

Regarding claim 1, Wang et al disclose an integrated circuit (IC) package comprising:

- an IC die (104 in Fig. 1) having a top side and bottom side opposite to the top side
- raised interconnects/bumps (not numerically referenced in Fig. 1) located over and conductively coupled to the die
- a flexible dielectric circuit film (FDCF)/interposer (100 in Fig. 1) having a top and bottom surfaces, the FDCF being made of a plurality of layers (120, 110, etc. in Fig. 1-3) including a routing conductor (layer 128 in Fig. 1 and 3), the FDCF having outer/inner landing/pad formed on the top/bottom surfaces respectively (inner landing 126 in Fig. 1-3; outer landing/pad -not numerically referenced in Fig. 1-3)

such that the outer/inner landings/pads are fully supported by the underlying/overlying circuit film respectively, the outer landing being laterally offset from the inner landing
- the inner and outer landings/pads being connected via the routing conductor in such a way as to form a staircase-shape/cantilever-like pattern/structure (Fig. 1), the routing conductor being integrally incorporated with the FDCF such that it is formed on a bottom surface of the dielectric film being embedded/wrapped inside the dielectric film (128/120 in Fig. 1-3) and further being connected to the top and bottom surfaces through conventional vias and pads (Fig. 1-3; Fig. 7a-8d; Col. 3-7)
- the FDCF being located over and conductively attached to the raised interconnects/bumps such that an air gap is formed between the IC die and the FDCF (Fig. 1), the FDCF being substantially of the same size as the die, and
- contact/external connection bumps (not numerically referenced in Fig. 1) conductively coupled to the outer landings/pads
(Fig. 1; 1-8d; Col. 3, line 29- Col. 6, line 65).

Wang et al disclose the conductive coupling of the die with the FDCF but fail to specify the top side of the die including at least one bond pad.

It is conventional in the chip packaging technology art to use an IC die having different configurations of bonding pads, terminals and electrodes on top/bottom

surfaces to achieve the desired external connections. The APA teaches the dice having such bond pads (Fig. 1A-3; specification pages 1-5).

Akagawa et al teach using a variety of conventional configurations where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the top side of the die including at least one bond so that the bond strength and reliability can be improved using the APA and Akagawa et al's pad structures in Wang et al's package.

Regarding claim 2, Wang et al disclose the air gap/height being equal to the height of the conventional connections/solder bumps but fail to specify the height being in a range of 10-500 microns.

The parameters such as air gap/spacing between the die and the substrate, bump height, bump/pad spacing/pitch/offset, size/dimension of the die/substrate, etc. in chip packaging and interconnection technology art are a subject of routing optimization to achieve the overall package size, reliability and interconnection/repair/test requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns so that the overall package size, reliability and interconnection/repair/test requirements can be achieved in Wang et al's package in view of Akagawa et al and APA.

Regarding claims 3, 6, 7 and 21-24, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claim 5, Wang et al further disclose the horizontal offset distance between the inner and outer landing/pad having different dimensions/ranges (see various power/ground landings/pads on the top/bottom surfaces of the FDCF in Fig. 1) and the same being a function of a number of variables such as chip electrode/pad pitch/spacing, signal/power line spacing, etc. (Col. 6, line 46- Col. 7, line 45) but Wang et al fail to specify the offset distance being in a range of 50-1000 microns.

As explained above for claim 2, the parameters such as, bump height, bump/pad spacing/pitch/offset, power/signal pad spacing/pitch, size/dimension of the die/substrate and air gap/spacing between the two, etc. in chip packaging and interconnection technology art are a subject of routing optimization to achieve the

power/signal routing, electrical performance, reliability and interconnection/repair/test requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the offset distance between the inner/outer landing being in a range of 50-1000 microns so that the power/signal routing and electrical performance/reliability can be improved and interconnection/repair/test requirements can be achieved in Wang et al's package in view of Akagawa et al and APA.

Regarding claim 15, as explained above for claim 1, Wang et al disclose the chip scale package (CSP) but fail to specify the IC die being a part of an IC wafer comprising a plurality of IC.

The APA teaches forming a variety of conventional IC packages which are singulated from a wafer comprising a plurality of IC die and are formed into a wafer scale package (WSP) or a CSP (specification pages 1-5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC die being a part of an IC wafer comprising a plurality of IC die so that the manufacturing yield and cycle time can be improved using Akagawa et al and APA's teachings in Wang et al's package.

Regarding claims 16, 17, 19, 20 and 25-28, the claim elements have been addressed in the rejections as explained above for claims 1, 2; 7, 5, 6 and 21-24 respectively.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7 and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

10-25-02

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800